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ABSTRACT OF THE DISCLOSURE

A Chip Scale Package (CSP) and a method of forming the same are disclosed. Single chips without the conventional ball mountings, are first attached to an adhesive-substrate (adsubstrate) composite having openings that correspond to the input/output (I/O) pads on the single chips to form a composite chip package. Ball mounting is then performed over the openings, thus connecting the I/O pads at the chip sites to the next level of packaging directly. In another embodiment, the adhesive layer is formed on the wafer side first to form an adwafer, which is then die sawed in CSPs. Then the CSPs with the adhesive already on them are bonded to a substrate. The composite chip package may optionally be encapsulated with a molding material. The CSPs provide integrated and shorter chip connections especially suited for high frequency circuit applications, and can leverage the currently existing test infrastructure.